

U.S. Patent Application Serial No. **09/765,437**  
Amendment dated August 8, 2003  
Reply to OA of **May 9, 2003**

### **REMARKS**

Claims 1-3, 5-16 and 18-26 are pending in this application, of which claims 7, 14 and 21 are withdrawn from consideration. Reconsideration of the rejections in view of these amendments and the following remarks is respectfully requested.

The claims have been amended in order to more particularly point out, and distinctly claim the subject matter to which the applicant regards as his invention. The applicant respectfully submits that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated May 9, 2003.

### **Rejections under 35 USC §102(b)**

**Claims 8, 10 and 11 were rejected under 35 USC §102(b) as being anticipated by Yamamichi et al (U.S. Patent No. 5,530,279).**

Claim 8 has been amended to recite “(a) forming a cup-shaped lower electrode above a semiconductor substrate formed with semiconductor elements, the lower electrode having a top surface and side surfaces.”

In Yamamichi et al, the lower electrode 104 is not cup-shaped. Thus, Yamamichi et al does not teach or suggest “(a) forming a cup-shaped lower electrode above a semiconductor substrate formed with

semiconductor elements, the lower electrode having a top surface and side surfaces,” as recited in claim 8.

Yamamichi forms ABO<sub>x</sub> type dielectric film by ion beam sputtering. In this process, the thickness of the dielectric film inevitably becomes thicker at the upper portion. Even after the milling process, the thickness at the shoulder portion may be thicker than the dielectric film at the lower portion. Here, it should be noted that Yamamichi does not positively thicken the film thickness at the shoulder portion. In a stack type capacitor, it is not necessary to thicken the dielectric film at the top portion.

In the cup-shaped cylindrical lower electrode, the top portion becomes thin. The dielectric film covers the lower electrode and the upper electrode is formed thereon. When a voltage is applied across the capacitor, electric field may concentrate at the top of the lower electrode. Therefore, it is necessary to strengthen the dielectric strength of the dielectric film at the top portion. Claims 10 and 11 clarify this situation. The step of forming a film with a good step coverage can form a dielectric film of uniform thickness. But, it is not enough to form a film of uniform thickness. The step of forming a film with a poor step coverage is positively employed to increase the thickness at the top portion.

For forming a cup-shaped cylindrical capacitor, it is difficult to use ion beam sputtering, because this method makes the deposited film thicker at the shoulder portion, also in the inside of the cup-shaped lower electrode, and may block the inside so that it becomes difficult to form a uniform upper electrode in the cylinder.

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For at least these reasons, claim 8 patentably distinguishes over Yamamichi et al. Claims 10 and 11, depending from claim 8, also patentably distinguish over Yamamichi et al for at least the same reasons.

**Claims 15 and 16 were rejected under 35 USC §102(b) as being anticipated by Lee (U.S. Patent No. 6,077,450).**

According to claim 15, the layers are formed from (1) a rare metal layer, (2) metal nitride layer, (3) an insulating mask layer, and (4) photo resist, in this order. Lee describes the process, at the portions referred to by the Examiner, as follows:

Referring initially to FIG. 3A, . . . . A 6000 Angstrom thick titanium nitride layer 24 is formed on the platinum layer 23. Instead of a titanium nitride layer 24, a titanium layer or an aluminum layer or an a aluminum alloy layer such as, Al/AlSi, or AlSiCu may be deposited. A **non-conductive layer such as a silicon oxide layer**, a silicon nitride layer, or a photoresist film may be additionally deposited on the titanium nitride layer 24.

Referring to FIG. 3B, a 7500 Angstrom thick photoresist film 25 is coated on the titanium nitride layer 24 and patterned selectively by using a KrF stepper having 0.43  $\mu\text{m}$  pitch (0.21 space).

Referring to FIG. 3C,  $\text{Cl}_2 + \text{HBr}$  is injected with the patterned photoresist film 25 serving as a mask to etch the titanium nitride layer 24. Then the remaining photoresist film is removed. **In case that a non-conductive layer is deposited on the titanium nitride layer 24, the non-conductive layer is etched with the patterned photoresist film serving as a mask and the titanium nitride layer 24 is then etched with the etched nonconductive layer serving as a mask.**

Referring to FIG. 3D, when the titanium nitride layer 24 serves as a mask, the platinum layer 23 is etched in 25  $\text{HBr} + 25 \text{O}_2$  under a pressure of 5 mTorr for 200 seconds by imposing an energy of 300-600 w (13.56

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MHz) on a high-frequency provider and an energy of 0-100 w (450 kHz)  
on a low-frequency provider.

The Examiner's allegation appears to be based on the layer formation (1) a rare metal (Pt) layer, (2) metal nitride (TiN) layer, (3) an insulating mask (non-conductive) layer, and (4) photo resist, in this order.

Claim 15, however, also recites "wherein said step (c) is **terminated before the rare metal layer is exposed**, wherein the resist pattern is removed before said step (d), and wherein said step (d) patterns the metal nitride layer and the rare metal layer by using the patterned insulating mask layer." Lee does not teach or suggest these recitations.

When a lamination of SiO<sub>2</sub>/TiN/Ru is etched using a resist mask, the resist should be removed before Ru surface is exposed. If the Ru surface is exposed before the resist mask is removed, by-product can be formed which cannot be removed after etching. Therefore, a hard mask is employed. The hard mask is patterned using a resist pattern, after the hard mask is patterned, the resist pattern is removed. In order to clarify this feature, claim 15 has been amended to recite "the resist pattern is removed before said step (d)."

For at least these reasons, claim 15 patentably distinguishes over Lee.

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**Rejections under 35 USC §103(a)**

**Claims 1-3, 5 and 22 were rejected under 35 U.S.C. §103(a) as being obvious over Saenger et al (U.S. Patent No. 5,633,781) in view of Alers (U.S. Patent No. 6,303,426).**

Admitting that Saenger et al does not specifically show heating the semiconductor substrate in a nitriding atmosphere to nitride the plug, the Examiner alleged that it would have been obvious . . . to modify Saenger et al reference by including the information provided by Alers in order to avoid oxidation on the surface of the bottom electrode and improved adhesion.

Claim 1 has been amended to recite “(d) forming a nitride etch layer by chemical vapor deposition including heating the semiconductor substrate and supplying nitride source gas to the semiconductor substrate, thereby nitriding the plug from a surface thereof; and forming a nitride layer on the first insulating film covering the nitrided plug surface.”

In Saenger et al, an electrically conductive diffusion barrier 8 is formed by a conventional process such as sputtering, and may be  $Ta_{1-x}Si_xN_y$  (with  $0 < x < 1$  and  $y > 0$ ), TiN, or similar materials (col. 4, lines 4-8). On the other hand, Alers teaches nitriding the exposed surface of the plug. Nothing in Saenger et al and Alers teaches nitriding the surface of W plug and simultaneously depositing a nitride layer.

Thus, the combination of Saenger et al and Alers does not teach or suggest, among other things, the step of “(d) forming a nitride etch layer by chemical vapor deposition including heating the semiconductor substrate and supplying nitride source gas to the semiconductor substrate, thereby nitriding

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the plug from a surface thereof, and forming a nitride layer on the first insulating film covering the nitrided plug surface.”

For at least these reasons, claim 1 patentably distinguishes over Saenger et al and Alers. Claims 2, 3, 5 and 22, all depending from claim 1, also patentably distinguish over Saenger et al and Alers for at least the same reasons.

**Claims 6 and 23 were rejected under 35 U.S.C. §103(a) as being obvious over Saenger et al in view of Alers, and further in view of Applicant's admitted prior art.**

Applicant's admitted prior art has been cited for allegedly disclosing forming the rare metal layer by sputtering followed by a CVD process using oxygen. Such disclosure, however, does not remedy the deficiencies of Saenger et al and Alers.

For at least these reasons, claims 6 and 23, depending from claim 1, patentably distinguish over Saenger et al, Alers and Applicant's admitted prior art.

**Claims 9, 12, 13 and 24 were rejected under 35 U.S.C. §103(a) as being obvious over Yamamichi et al in view of Applicant's admitted prior art.**

As discussed above, claim 8 patentably distinguishes over Yamamichi et al. Applicant's admitted prior art has been cited for allegedly disclosing forming the rare metal layer by sputtering followed by a

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CVD process using oxygen. Such disclosure, however, does not remedy the deficiencies of Yamamichi et al.

For at least these reasons, claims 9, 12, 13 and 24, depending from claim 8, also patentably distinguish over Yamamichi et al and Applicant admitted prior art.

**Claims 18-20 and 26 were rejected under 35 U.S.C. §103(a) as being obvious over Lee in view of Joo (U.S. Patent No. 6,342,425).**

As discussed above, claim 15, from which claim 18 depends, patentably distinguishes over Lee. Joo has been cited for allegedly disclosing forming dielectric film on the patterned lower electrode. Such disclosure, however, does not remedy the deficiencies of Lee.

For at least these reasons, claims 18-20 and 26, depending from claim 15, also patentably distinguish over Lee and Joo.

**Claim 25 was rejected under 35 U.S.C. §103(a) as being obvious over Lee in view of Joo and Hasegawa et al (U.S. Patent No. 6,452,274).**

Claim 25 recites, among other things, “(f) forming an insulating film over the semiconductor substrate, the insulating film covering the patterned insulating mask layer.” That is, the patterned insulating mask layer is used in the semiconductor device.

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In Lee, the nitride layer (24) is removed after etching the platinum layer 23 and not used in the semiconductor device. Joo is cited for allegedly disclosing forming a dielectric film over the semiconductor substrate, but such disclosure in Joo does not remedy the deficiency of Lee.

Hasegawa has been cited for allegedly disclosing TaO being used instead of silicon oxide as a mask as conventional in the art. If a TaO layer is used for patterning the low-k film and is used in the semiconductor device, the effect of low-k film should be lessened by the existence of TaO film which has a high dielectric constant. Those skilled in the art would not think of using a high dielectric constant material adjacent to the low-k film. Whereas on the upper electrode of a capacitor, a high dielectric constant layer may pose no problem, and may not be removed.

For at least these reasons, claim 25 patentably distinguish over Lee, Joo and Hasegawa et al.

In view of the aforementioned amendments and accompanying remarks, claims as amended, are in condition for allowance, which action, at an early date, is requested.

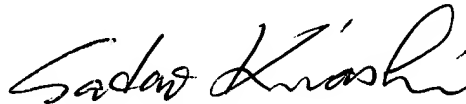
If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

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In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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